Amendments to the Claims

Claims 1 – 8 are pending in this application with claims 1, 2, 4 and 6 – 8 being amended, new claims 9 – 11 being added and claim 3 being cancelled by this response.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of the Claims

1. (Currently Amended) A video apparatus with a digital decoder ~~having~~ comprising:

a first memory ~~on an internal bus and linked to~~ for storing video data;

a second memory for storing on-screen display data;

an on-screen display ~~OSD~~ circuit for generating on-screen display graphics signal from the on-screen display data in the second memory;

wherein the first memory is adapted to receive on-screen display data that is no longer being displayed from the second memory and to transfer said on-screen display data back to the second memory in response to a request for display of data stored in the first memory

~~and to a second memory via a main bus,~~

~~the video apparatus comprising means for realising a DMA transfer between the first memory and the second memory~~.

2. (Currently Amended) A video apparatus according to claim 1, ~~wherein a CPU is connected to the main bus~~ further comprising a processing unit, the first memory not being directly accessible by the processing unit.

3. (Cancelled)

4. (Currently Amended) A video apparatus according to claim 1, wherein the first memory is a ~~Video RAM and wherein the second memory is CPR RAM~~ random access memory used for video decompression.

5. (Original) A video apparatus according to claim 1, wherein the digital decoder is connected to a digital front-end.

6. (Currently Amended) A process for controlling a video apparatus ~~with~~ comprising a digital decoder ~~having,~~ a first memory, a second memory ~~on an internal bus and linked to~~ and an on-screen display ~~OSD~~ circuit ~~and to a second memory via a man bus, comprising the step of realising a DMA transfer between the first memory and the second memory via the digital decoder.~~ for generating an on-screen display signal based on data stored in the second memory, said method comprising the steps of:

writing on-screen display data to the second memory for access by the on-screen display circuit;

wherein, the first memory is used for video decompression, further comprising the steps of:

-transferring on-screen display data that is no longer being be displayed to the first memory; and

-upon request, transferring back on-screen display data from the first memory to the second memory.

7. (Currently Amended) A process according to claim 6, further comprising the ~~following~~ steps of:

- issuing a request for the ~~OSD~~ on-screen display circuit to use more than a given size in the second memory,

- ~~realising~~ realizing a ~~DMA~~ direct memory transfer of on-screen display data from the second memory to the first memory.

8. (Currently Amended) A process according to claim 7, ~~with the~~ further comprising the steps of:

- issuing a request for the ~~OSD~~ on-screen display circuit to use on-screen display data in the first memory, and

~~- copying via a DMA transfer data from the second memory to the first memory;~~

- ~~realising a DMA transfer~~ transferring said on-screen display data to be used ~~of the requested data~~ from the first memory to the second memory.

9. (New) A process according to claim 7, wherein the transfer of on-screen display data to the first memory occurs when the first memory is unavailable for video decompression.

10. (New) A video apparatus according to claim 1, wherein transfer between the first and second memories is made using a direct memory access.

11. (New) A video apparatus according to claim 4, wherein the first memory is made available for storing on-screen display where the first memory is not being used for holding video data.